EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L2	720	((first adj2 logic with register) same (second adj2 logic with register)).CLM.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/11/04 13:34
L3	231	((first adj2 logic with register with control$4) same (second adj2 logic with register with control $4)).CLM.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/11/04 13:35
L4	1	((first adj2 logic with register with control$4) same (second adj2 logic with register with control $4) and (timing adj verification)).CLM.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/11/04 13:36
L5	2	((first adj2 logic with register with control$4) same (second adj2 logic with register with control $4) and (timing adj verification))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/11/04 13:36
L6	64	(core with register with buffer).CLM.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/11/04 13:37
S1	488	"716"/$.CCLS. and (first adj2 logic) same (second adj2 logic)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/04/03 06:14
S2	85	"716"/$.CCLS. and ((first adj2 logic) same (second adj2 logic) same (register flip$1flop latch)) and @ad<"20060427"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/04/03 06:15
S3	52	"716"/$.CCLS. and ((first adj2 logic) with (second adj2 logic) with (register flip$1flop latch)) and @ad<"20060427"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/04/03 06:33

S4	6	"716"/$.CCLS. and ((first adj2 logic) with (second adj2 logic) with (register flip$1flop latch) with control) and @ad<"20060427"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/04/03 06:37
S5	576	((first adj2 logic) with (second adj2 logic) with (register flip$1flop latch) with control) and @ad<"20060427"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/04/03 06:42
S6	4	((first adj2 logic) with (second adj2 logic) with (register flip$1flop latch) with control) and @ad<"20060427" and (timing with verification)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/04/03 06:43
S7	0	"716"/$.CCLS. and (two adj stage adj design) and @ad<"20060427"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/04/03 07:14
S8	4	"716"/$.CCLS. and ((first adj2 logic) same (second adj2 logic) same control same verification)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/04/03 07:15
S11	35	"716"/$.CCLS. and (logic adj verification) and (timing adj verification)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/04/03 08:51
S12	33	("5801958" | "5903475" | "6009256" | "6094726" | "6269467" | "6304837" | "6360353" | "6532561"). PN. OR ("6678645"). URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2008/04/03 09:16
S13	154	"716"/$.CCLS. and (macro with registers)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/04/03 09:50
S14	111	"716"/$.CCLS. and (macro with registers) and @ad<"20031031"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/04/03 09:52

S15	10	"20020083398" "20030009727" "20040232459" "20040238827" "20050250266"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/04/03 10:09
S16	13	("6995432" "6955954" "6697059" "6678871" "6624445" "6489632" "6400360" "6034675").pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/04/03 10:13
S17	24	"716"/$.CCLS. and (macro with registers with buffer) and @ad<"20031031"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/04/07 08:26
S18	18	"716"/$.CCLS. and (registers with I/O adj buffer) and @ad<"20031031"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/04/07 08:32
S19	23	"716"/$.CCLS. and ((flip $1flop latch register) with I/O adj buffer) and @ad<"20031031"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/04/07 08:40
S20	127	"716"/$.CCLS. and ((flip $1flop latch register) with (input output I/O) adj buffer) and @ad<"20031031"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/04/07 09:11
S21	24	(core with register with buffer) and "716"/$.CCLS.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/04/07 09:50
S22	2472	716/5.CCLS.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/04/07 14:51
S23	1884	716/1.CCLS.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/04/07 14:51
S24	1949	716/6.CCLS.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/04/07 14:51

S25	2	"20070130550"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/09/16 07:48
S26	14	((first adj2 logic) same (second adj2 logic) same control same verification).CLM.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/09/16 07:51
S27	1	((first adj2 logic) with (second adj2 logic) with (register flip$1flop latch) and layout and verification).CLM.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/09/16 07:52
S28	0	((logic adj verification) and (timing adj verification)).CLM.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/09/16 07:53
S29	63	(core with register with buffer).CLM.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/09/16 07:54
S30	2	"20070093029"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/09/16 10:24

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